WHITE PAPER

Signal Integrity Fundamentals

From simulation to measurement

Data centers depend on channels in transmit and receive systems to accurately and efficiently deliver valuable information. A poorly performing device in a channel can cause signal integrity issues and jeopardize the delivery of intelligible data. That makes developing channel devices and interconnects with high signal integrity critical. Testing and identifying the sources of signal integrity issues in a device, then fixing them, is a big challenge. This paper includes simulation and measurement recommendations to help you design your device for high signal integrity.

A central processing unit (CPU) that sends information to a light-emitting diode display is a good example of a digital communications channel. The channel — everything between the CPU and the display — includes interconnect devices such as a graphics card, cables, and an onboard video processor. Each device, as well as the connections between them in the channel, creates opportunities for disturbance or interference to the CPU's transmitted data.

Signal integrity problems may include cross talk, delays, ringing, and electromagnetic interference. Addressing signal integrity problems early enables the development of high-performance products with higher reliability and lower costs.

Highlights in this paper include:

- Channel simulation
- Determining the root cause of signal degradation
- Exploring and designing signal integrity solutions
- Signal integrity measurement analysis

KEYSIGHT TECHNOLOGIES

Channel Simulation

Engineers use electronic design automation software to create a circuit simulation. Design automation software provides fast and accurate channel simulation using bit-by-bit and statistical simulation technology. An algorithmic modeling interface is a standard used in design software to provide easy simulation of multi-gigabit serial links (transmit to receive).

Engineers use signal analysis tools such as the eye diagram, mixed-mode S-parameters, time-domain reflectometry, and single pulse response, in addition to the simulation software. While simulating data transmission from the transmitter to the receiver, the eye diagram that an oscilloscope displays is the analysis tool that helps evaluate a channel's performance.

Within the diagram, eye width and height are key indicators of signal distortion. A wide-open eye means the transmitted data is good. A closed eye indicates signal integrity degradation. If the eye diagram shows an open eye at the transmitter and a closed eye at the receiver, the next step is to determine which devices or interconnects in the channel are causing the signal degradation. View the eye diagram directly at the transmitter's output and progress through each interconnect up to the receiver to determine which device is responsible for degrading the signal.

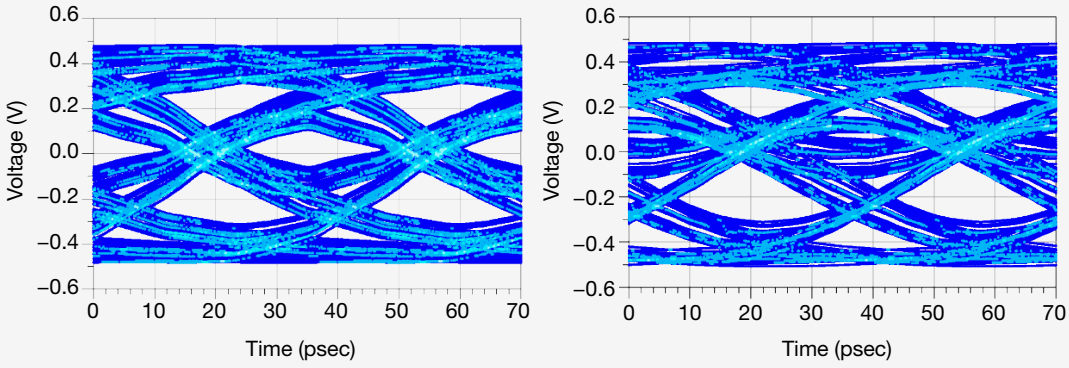

Figure 1: Example of an open eye (left) and a closed eye (right)

Determine the Root Cause of Signal Degradation

S-parameters are the de facto standard for engineers to describe the frequency behavior of a given device. The S-parameters of an interconnect, whether measured in the time domain or the frequency domain, represent a behavioral model of the interconnect. They contain all the information about how a signal entering one port will behave when it exits another port.

To determine the root cause of signal degradation, it is important to first determine the expected values of the S-parameters. Comparing the expected values to the measured values will help identify the channel area that is causing signal integrity degradation.

Next, take a deeper look into the device or interconnect to determine the root cause. For differential channels, determine root cause by using mixed-mode S-parameters for analysis. Differential return loss (SDD11), differential insertion loss (SDD21), and differential-to-common-mode conversion (SCD21), which relate to electromagnetic interference, are the most common S-parameters.

Refection is also important to consider when analyzing transmission quality. Whenever there is an instantaneous impedance change, the discontinuity will create a reflection. A reflection can mirror the original signal back with a delay, as shown below in Figure 2, causing destructive interference when combined with the original signal.

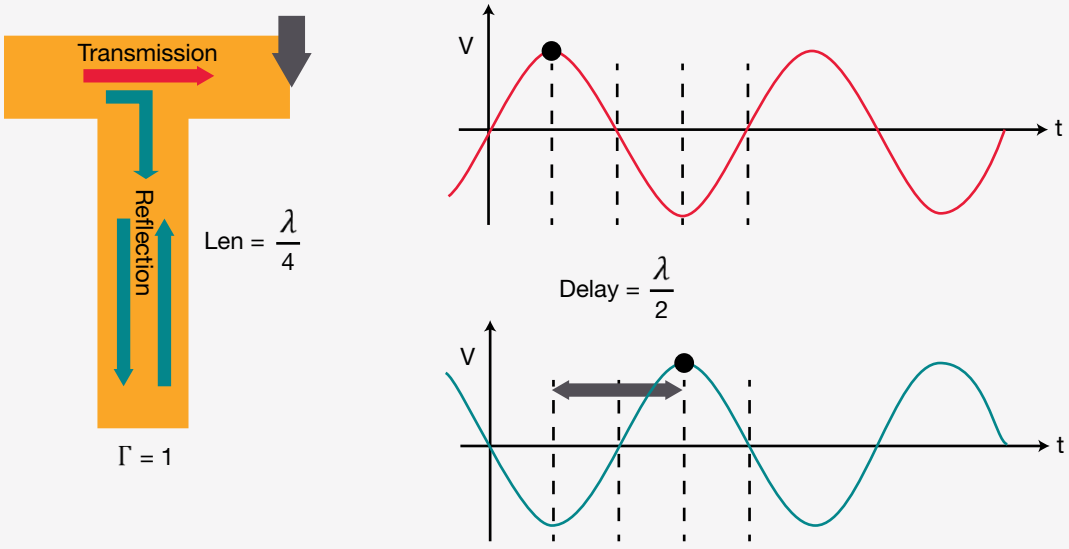

Figure 2: Effects of reflection on signal quality

Explore and Design Signal Integrity Solutions

Once you discover the signal degradation's root cause, you need to explore possible fixes and identify the best solution. Begin by using simulation to test the removal of the offending part of the design and verify that you have found the signal integrity degradation's root cause. Rather than removing the offending area as a solution, explore adding equalization, such as decision feedback equalization (DFE), continuous time linear equalization in the frequency domain, or transmitter feed-forward equalization in the time domain, at the receiver. Once again, use simulation to add the equalization and test if it has fixed the signal integrity degradation by looking for the open eye on an oscilloscope.

Applying an eye mask before and after applying the equalization, as shown in Figure 3, is another test option. Before you add equalization, the images intersect, indicating a closed eye. After you apply equalization, the images no longer intersect, indicating an open eye.

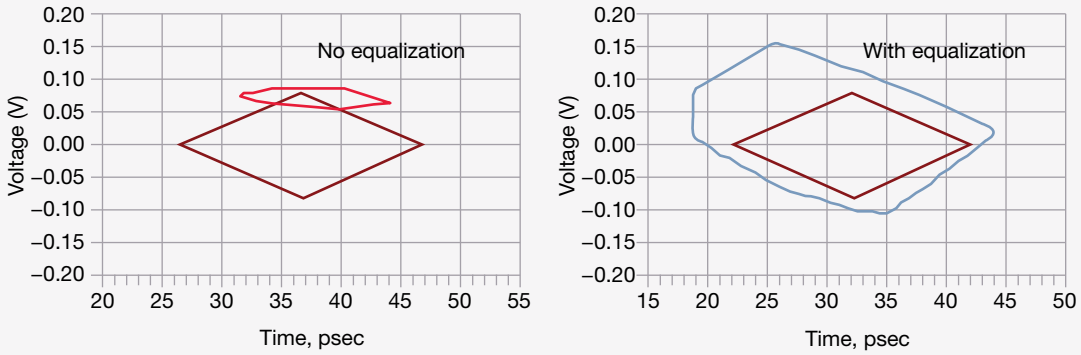

Figure 3: Eye mask comparison before and after applying DFE

Signal Integrity Measurement Analysis

As your product design progresses from simulation to hardware, you will need a vector network analyzer (VNA) to test the high-speed digital interconnects. Start by having a good idea of what measured results you expect for the channel, physical layer device, connector, cable, backplane, or printed circuit board. This information will provide comparison values once you acquire the measurement results. The goal is to establish a robust signal integrity workflow with both the software and the hardware. The hardware measurement steps include instrument measurement setup, acquiring channel data, and analyzing the channel performance.

For a high-dynamic-range instrument such as a VNA, it is important to understand error correction to ensure the most accurate S-parameter measurements. Error correction includes both calibration (a pre-measurement error correction) and de-embedding (a post-measurement error correction). The calibration and de-embedding reference points are adjusted to remove all items in the channel except for the device under test (DUT). The following information describes the differences between the calibration and de-embedding error corrections and how to use them.

Calibration

When you power up a VNA, by default the reference plane is at the front panel. When you add the cables needed to connect to the DUT, the calibration reference must move to include the cables using short open load through (SOLT), through reflect line, or through reflect match reference structures. SOLT is the most common method.

The cables may connect directly to the DUT or to a fixture. A fixture, installed between the cables and the DUT, helps accommodate different types of connectors, such as HDMI, display port, serial ATA, and PCI Express. For this example, the calibration reference plane includes the cables, and the de-embedding reference plane includes the fixture. The combined error correction of calibration and de-embedding must include all interconnects in the channel right up to the DUT. Once you connect the DUT, you can make the measurements and perform the post-measurement (de-embedding) error corrections.

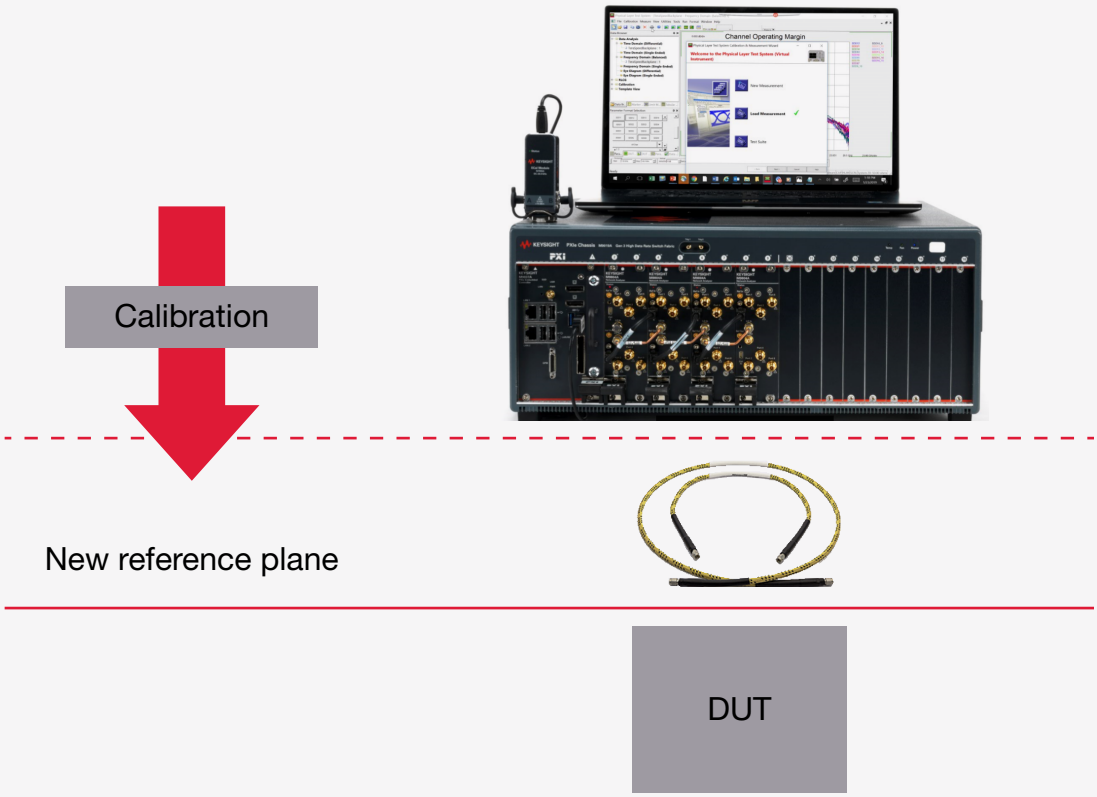

Figure 4: Calibration test setup with reference plane

De-embedding

After making the measurements, set the de-embedding reference points at the input and the output of the DUT to remove the test fixture. Removing the test fixture eliminates loss and reflections it introduced into the system, resulting in accurate S-parameter measurements and representation of the device.

By comparing the two-tier (calibration and de-embedding) correction S-parameter results to the expected results, you can make model adjustments to match the actual measurements and continue the device development.

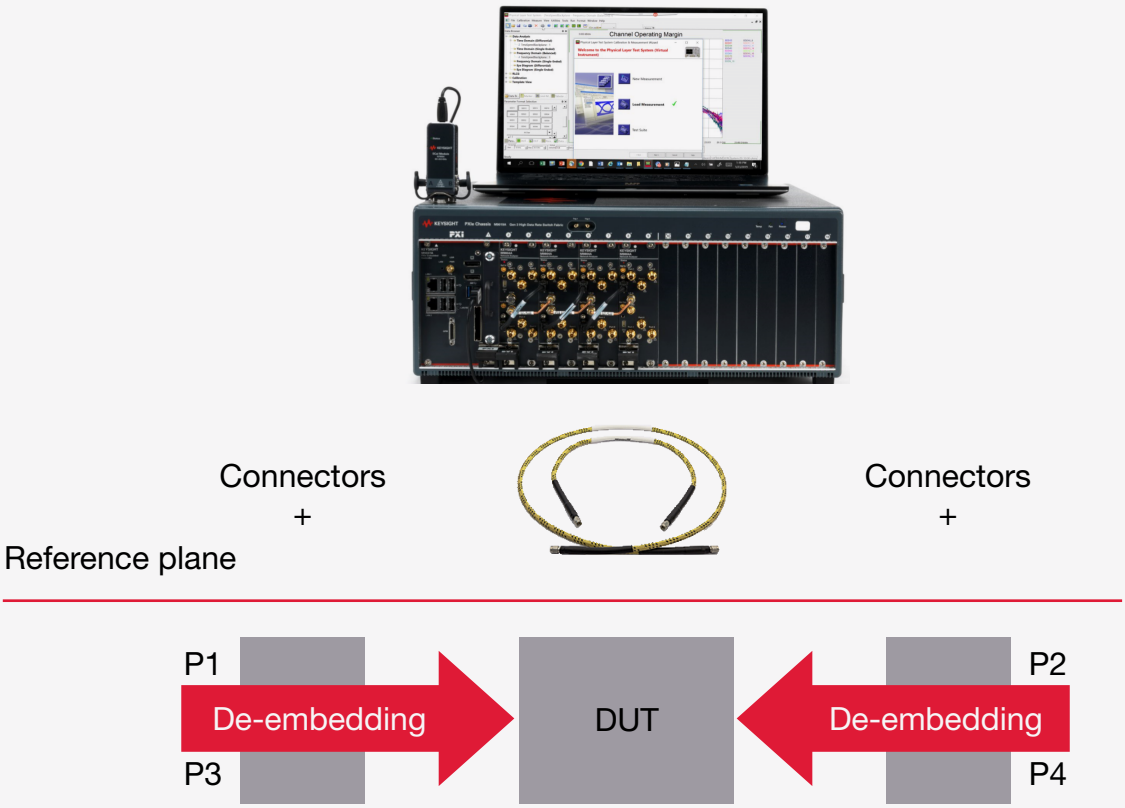

Figure 5: De-embedding test setup with reference plane

Solving Signal Integrity Issues

As transmitted data speeds increase, high signal integrity has become vital for channel devices and interconnects. To ensure high signal integrity for your device, start by determining the simulation and measurement results you expect to see and compare them to the measured results.

Next, use a combination of signal analysis techniques, like the eye diagram displayed on an oscilloscope, and simulation software to determine the root cause of signal degradation. Once you have designed a solution to address the signal integrity issues, you will need to establish a robust signal integrity workflow with both the software and the hardware.

Using a qualified VNA, set the calibration reference plane, make the S-parameter measurements, and set the de-embedding reference planes to properly remove the fixture. The results will include accurate S-parameters and a reliable representation of the device. By addressing signal integrity problems early, you optimize circuit design and ensure your devices work reliably at a reasonable cost.

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